CLAIMS

1. A semiconductor memory device comprising:

a memory cell region, including a first transistor provided on a principal surface of a semiconductor substrate; and

a logic circuit region, including second and third transistors of mutually different conductivity types,

wherein on a principal surface of a first insulating film above said first, second and third transistors, a first wiring made of a first metal is formed in a memory cell region and a logic circuit region, and wherein said first wiring is connected to said first, second and third transistors through a connecting body, including first conductors provided in openings passing through said first insulating film.

2. A semiconductor memory device according to Claim 1, wherein said semiconductor substrate is made of silicon, and wherein the properties of said first conductor and first metal are such that said first conductor does not increase contact resistance by reaction with said silicon and that said first conductor is lower in etching rate than the first metal.

3. A semiconductor memory device according to Claims 1 and 2, wherein said first conductor and said first metal are mutually different high refractory metals.

4. A semiconductor memory device according to Claims 1 to 3, wherein said first conductor is titanium nitride or titanium-tungsten, and wherein said first metal

is tungsten.

5. A semiconductor memory device according to Claim 1, wherein said first conductor is connected through a silicide layer to said silicon substrate.

6. A semiconductor memory device according to Claim 1, wherein a source region, a drain region and a gate electrode of each of said first, second and third transistors are connected through a connecting body including said first conductor to said first metal.

7. A semiconductor memory device having a memory cell, including a first transistor on a principal surface of a silicon substrate and a first wiring formed by a first metal, said first wiring being laid through a first insulating film and a second insulating film above said first transistor, wherein a first element is formed on said first wiring through a third insulating film, and wherein said first element is connected to said first transistor through a connecting body including a first conductor provided in an opening passing through said first insulating film, and a second conductor provided in an opening passing through said second insulating film and a third insulating film.

8. A semiconductor memory device according to Claim 7, wherein said first conductor and said second conductor are substantially cylindrical, and wherein said first conductor is electrically insulated from said gate electrode by fourth and fifth insulating films formed at sidewalls and a top of said gate electrode of said first

transistor, wherein a part of said first conductor is so arranged as to overlie said gate electrode of said first transistor and a sixth insulating film for isolation, and wherein an average diameter of said second conductor is smaller than an average diameter of said first conductor.

9. A semiconductor memory device according to Claim 1, wherein a width of said first wiring is smaller than an average diameter of said first conductor at the opening passing through said first insulating film.

10. A semiconductor memory device according to Claim 1 or 7, wherein said first wiring is the data line of a dynamic random access memory cell, and wherein said first element is a capacitor of a dynamic random access memory cell.

11. A semiconductor memory device according to Claim 7, wherein said first element is a polysilicon transistor of a static random access memory cell, and wherein said first wiring is power supply wiring of said static random access memory.

12. A semiconductor device according to Claim 11, wherein said first wiring is local wiring connecting gate electrodes or source and drain regions of transistors of mutually different conductivity types.

13. A semiconductor device comprising a memory cell including a first transistor provided on a principal surface of a silicon substrate, and a logic circuit including second and third transistors of mutually different conductivity types, wherein on a principal

surface of a first insulating film, a plurality of first wirings made of a first metal are formed in a memory cell region and a logic circuit region, wherein said first wirings are connected to said first, second and third transistors by connecting body including said first wiring and passing through said first insulating film, wherein a second insulting film is provided on said first wiring, wherein a first element is provided on a principal surface of said second insulating film in the memory cell region, and wherein said first element is connected to said first transistor by a connecting body including said first conductor and second conductor penetrating into said second insulating film.

14. A semiconductor device according to Claim 13, wherein said second conductor is formed of titanium nitride.

15. A semiconductor memory device according to Claim 1, further comprising a pair of inverters, each including said second and third transistors; a latch-type flip-flop circuit formed by said pair of inverters; a pair of signal lines connected to said flip-flop circuit; and first and second switching transistors formed by said second or third transistors, wherein a connecting body having the gate of each of said pair of inverters connected to the drain of the other inverter in cross connection includes said first wiring and said first conductors.

16. A semiconductor integrated circuit device having a first insulating film provided on a principal surface of

a semiconductor substrate and a first wiring formed by a conductor filled in a first opening in said first insulating film, wherein insulating side walls formed of other insulating films are deposited on side walls of said first opening of said first insulating film and a line width of said first wiring is defined by said side walls.

17. A semiconductor integrated device according to Claim 16, wherein said first wiring is formed by a high refractory metal.

18. A semiconductor integrated device according to Claim 16, wherein said first wiring has a sectional contour of an inverted taper.

19. A semiconductor integrated device according to Claim 16, wherein said fourth insulating film is silicon nitride.

20. A semiconductor integrated circuit device according to Claim 16, wherein on said semiconductor substrate, there are formed a latch-type flop-flop circuit formed by a pair of inverters connected to a pair of signal lines; first and second switching transistors connected to respective signal lines; first power supply wiring; second power supply wiring; and control lines connected to said first and second switching transistors, either of said first and second power supply wirings and either of said first and second control lines include at least said first wiring.

21. A semiconductor integrated circuit device according to Claim 16, wherein on a principal surface of

said semiconductor substrate, there is formed a dynamic random access memory, including a memory cell formed by a switching transistor and an electric charge storage capacitor connected to said switching transistor; a word line for selecting said switching transistor; and a data line for reading and writing information, wherein said data line is formed by said first wiring.

22. A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

forming a MISFET on a semiconductor substrate;

depositing a first insulating film;

etching a desired region in said first insulating film and forming a first opening for a wiring pattern;

depositing a sixth insulating film and forming sidewall spacers formed by said seventh insulating film at sidewalls of said first opening by anisotropic etching; and

depositing a first conductor in said first opening.

23. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

forming a MISFET on a MISFET on a semiconductor substrate;

depositing a first insulating film on said MISFET;

depositing a platinum film on said first insulating film;

depositing amorphous silicon on said platinum film and dry etching the amorphous silicon at a desired region;

forming platinum silicide at that region on said platinum film where there is amorphous silicon, by heat treatment; and

removing said platinum silicide by wet etching to therey leave a platinum electrode intact at a desired region.

24. A method of manufacturing a semiconductor integrated circuit device according to Claim 23, wherein said platinum electrode is an electrode of a capacitor of a dynamic random access memory cell, said capacitor electrode being formed raised on the principal surface of the semiconductor substrate.